

FIG. 1

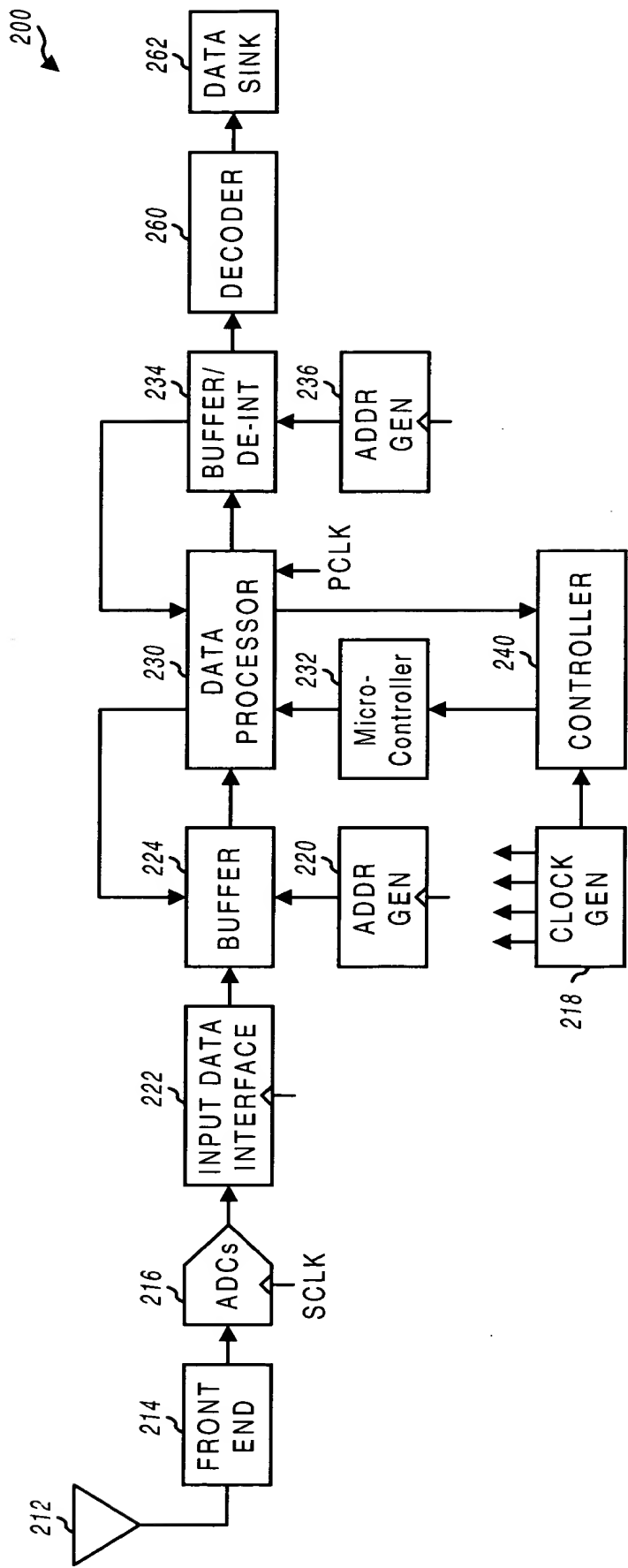


FIG. 2

FIG. 3 is a block diagram of a slot structure in a TDMA system.

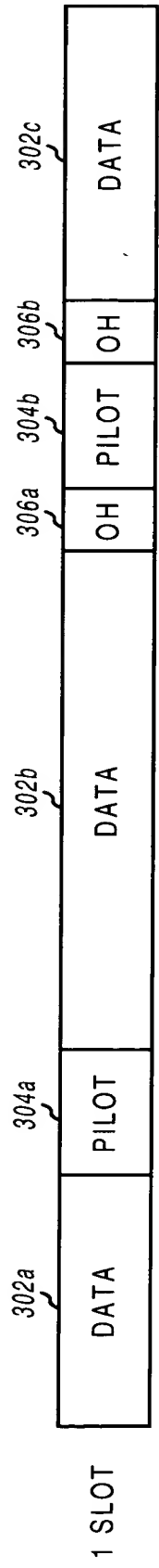


FIG. 3

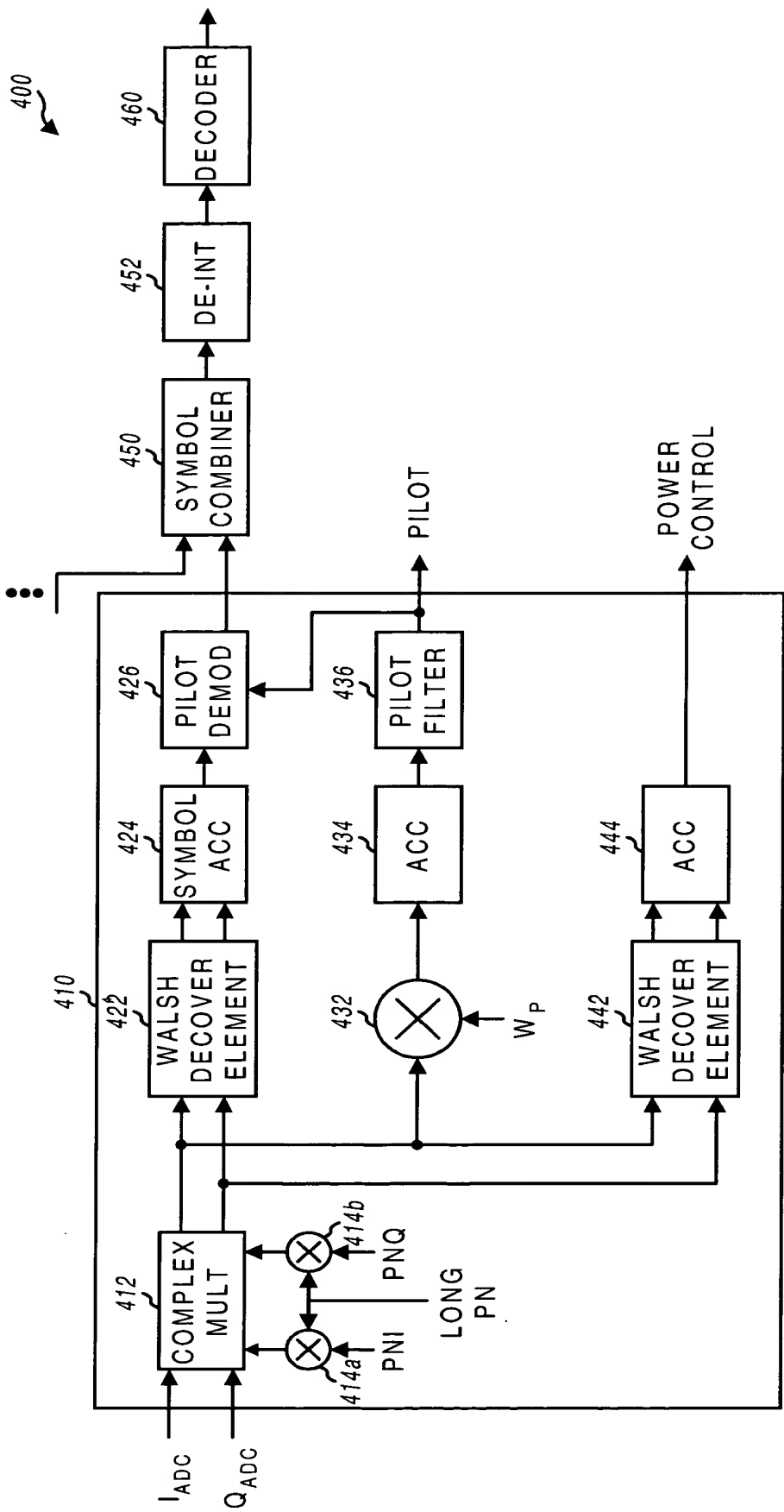


FIG. 4

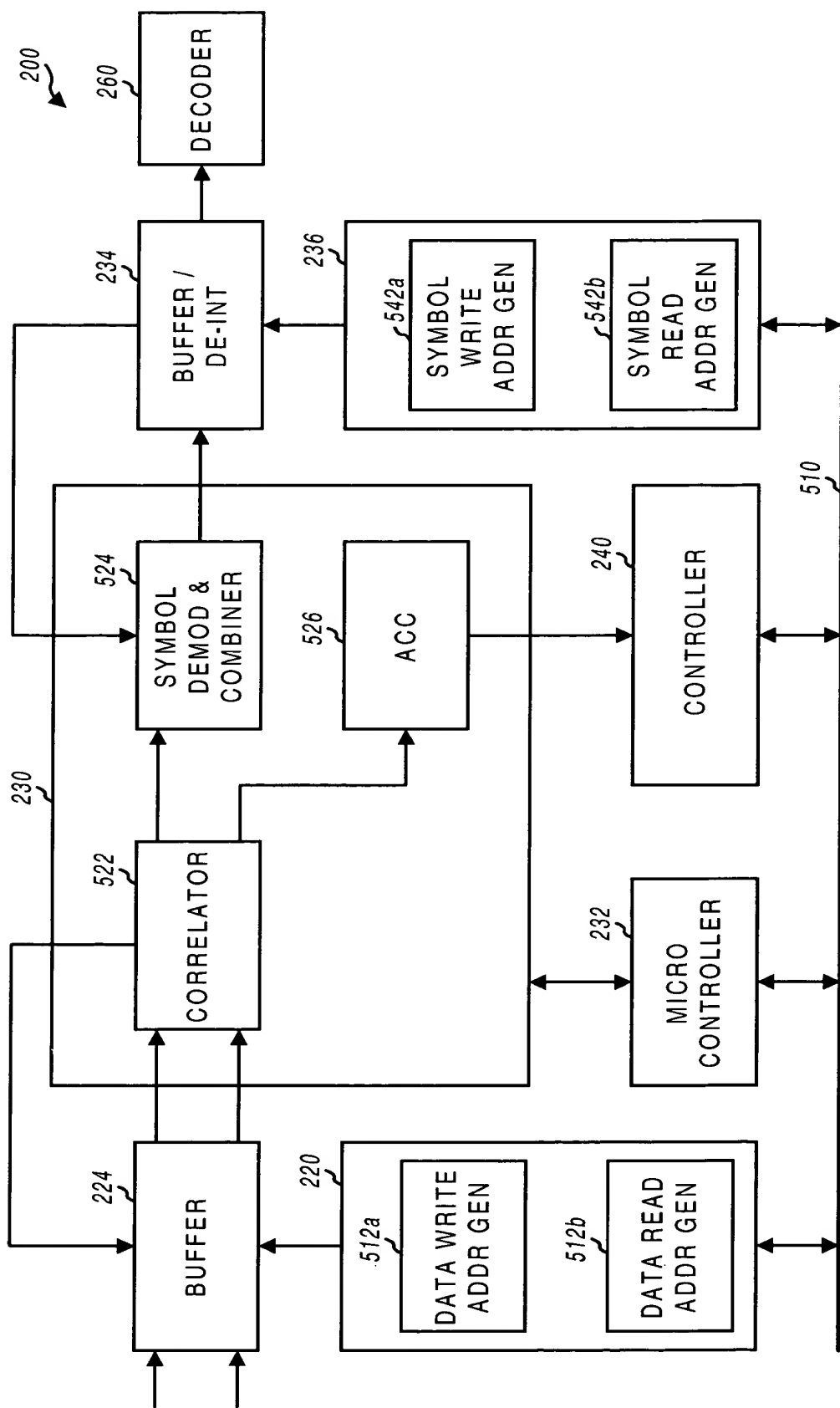


FIG. 5

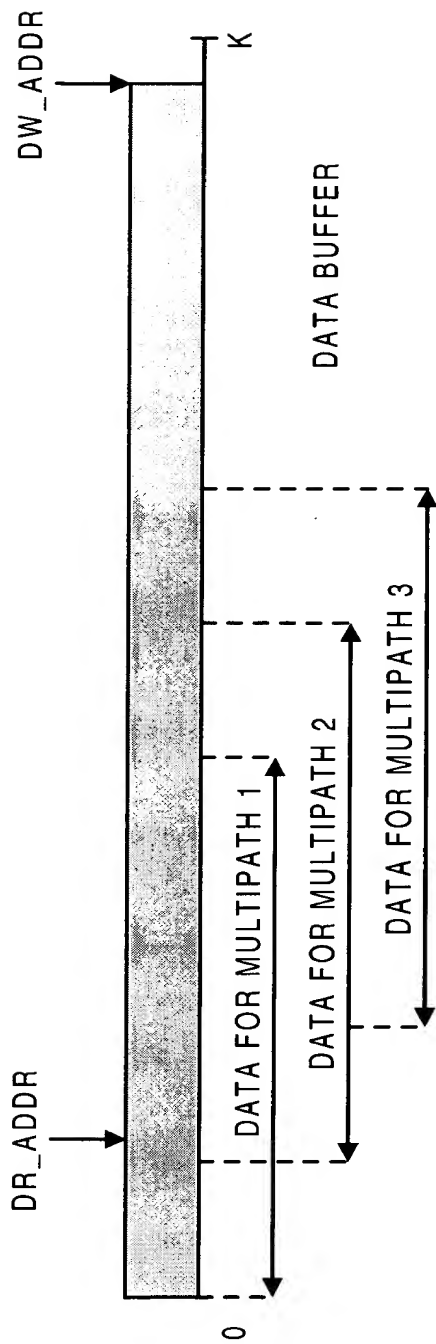


FIG. 6A

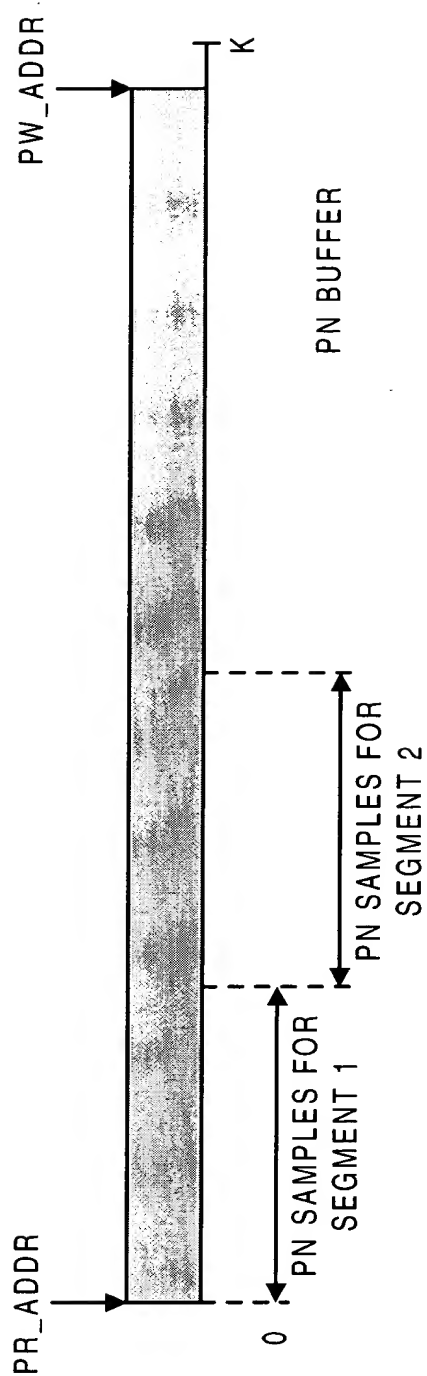


FIG. 6B

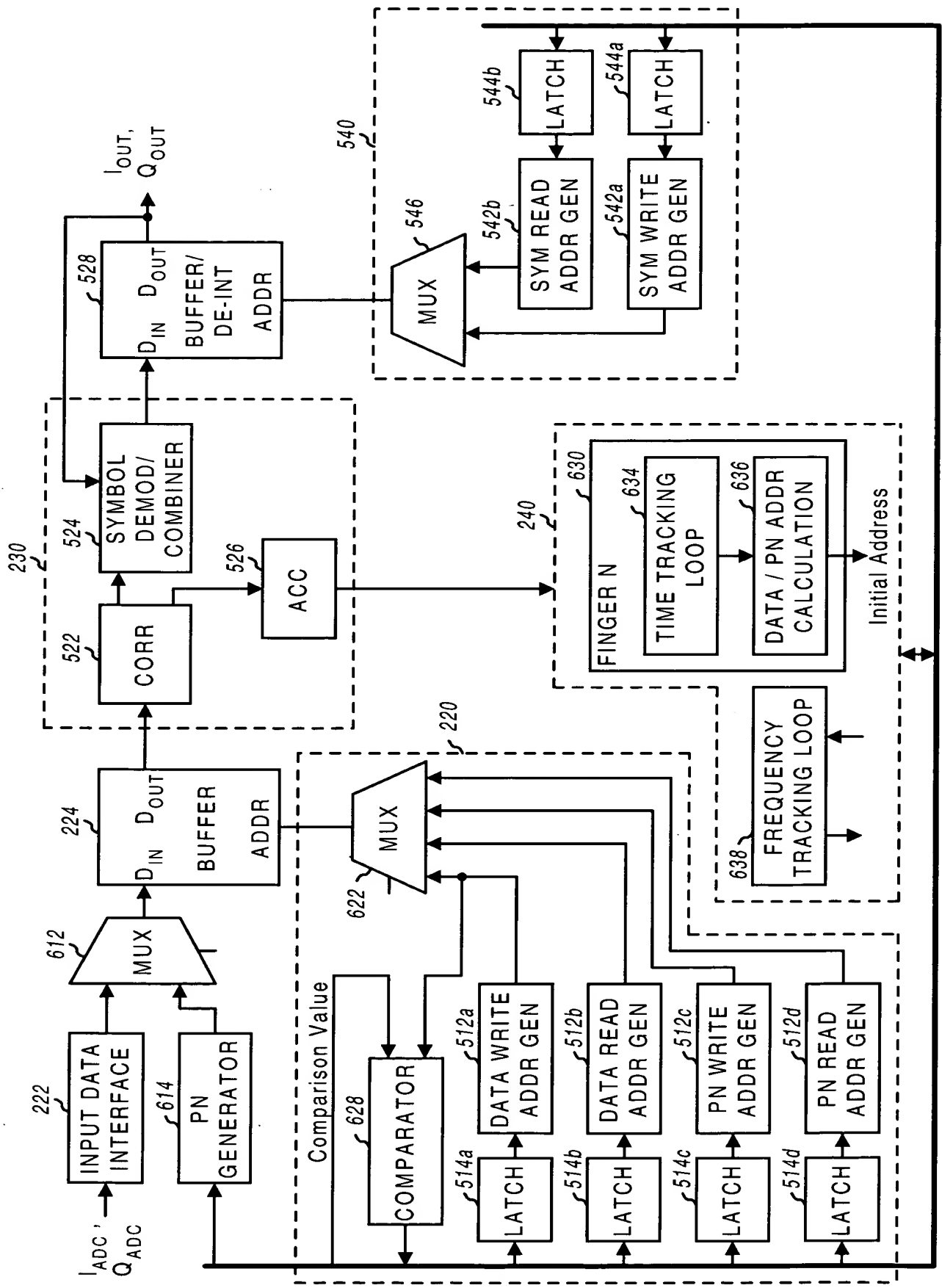


FIG. 6C

FIG. 7A is a block diagram of a digital signal processing system, such as a digital filter, according to one embodiment of the present invention.

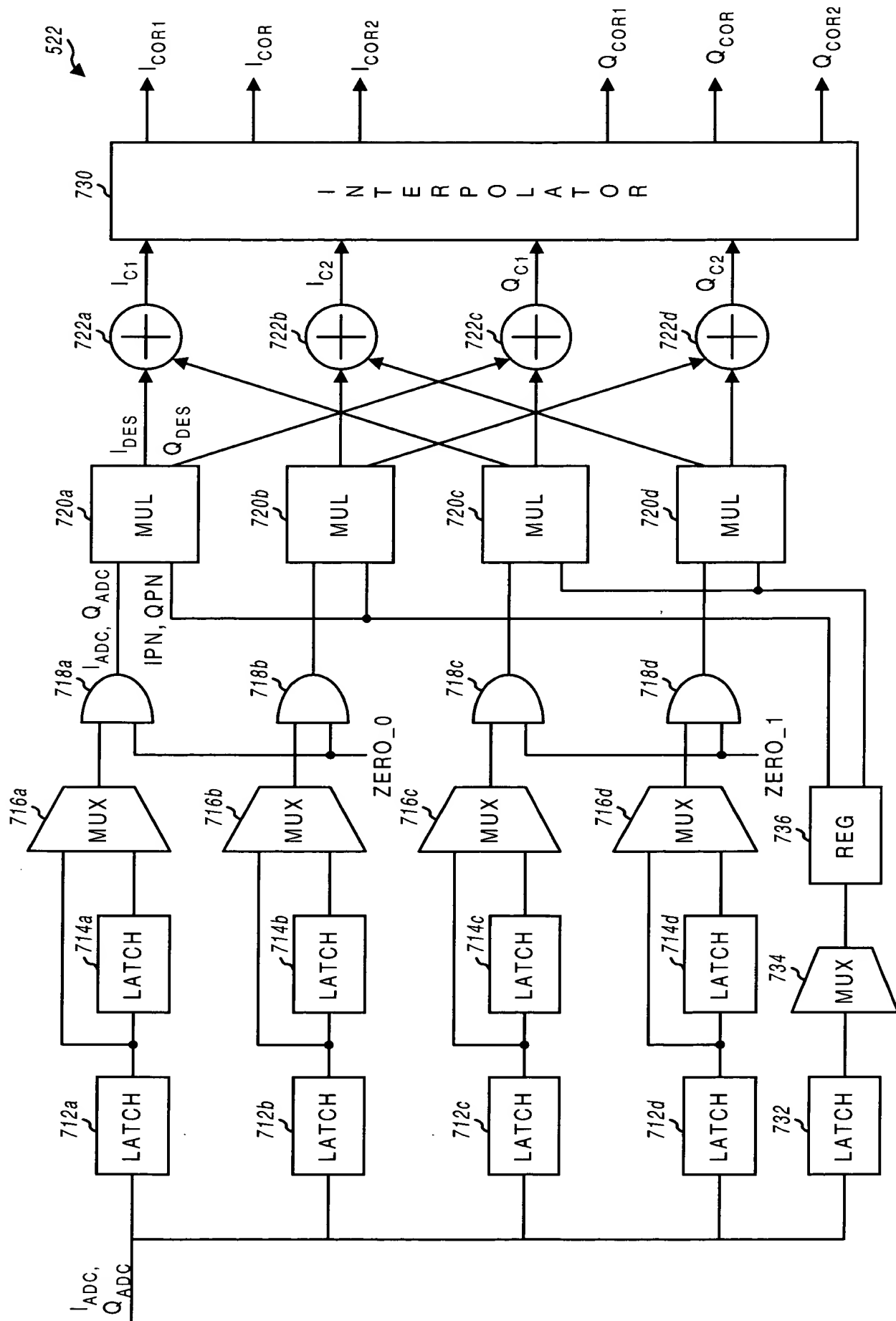


FIG. 7A



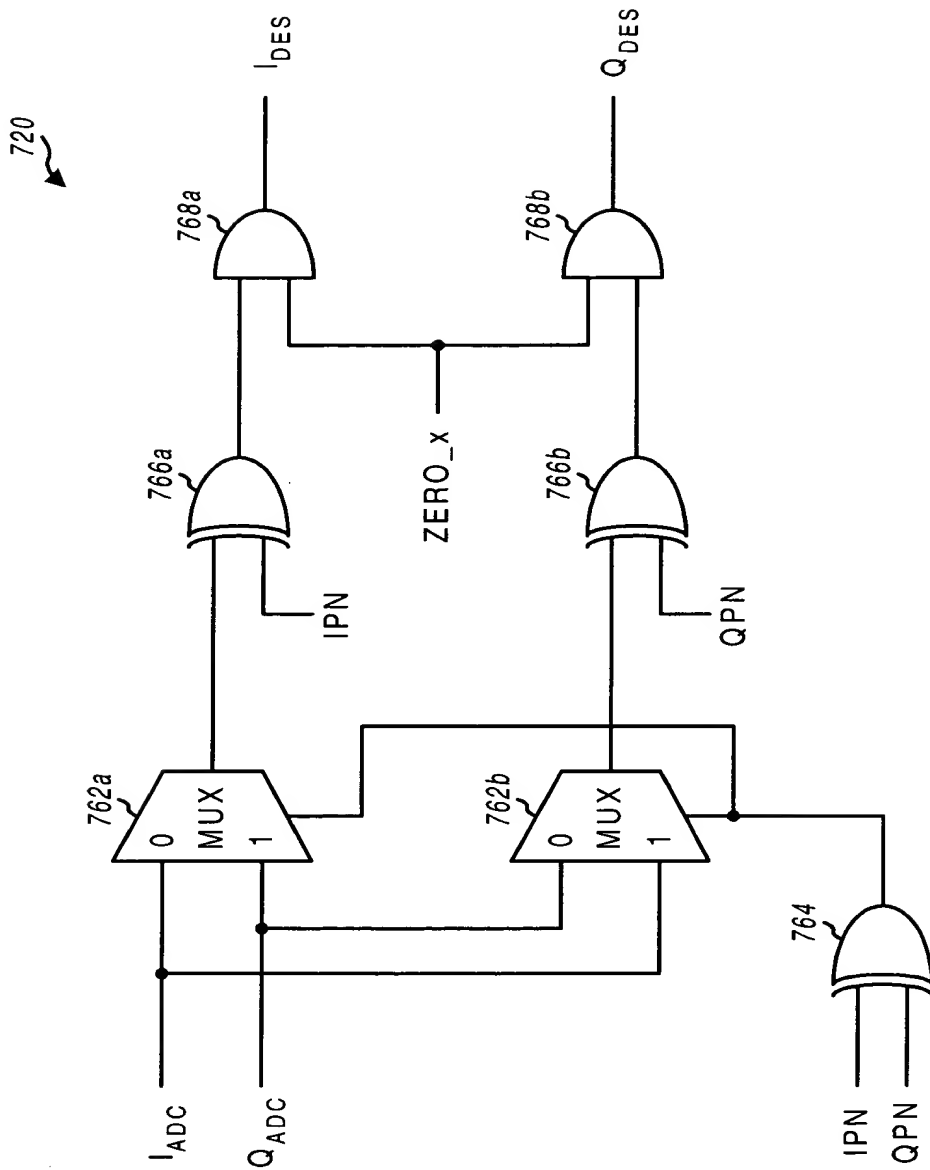


FIG. 7B

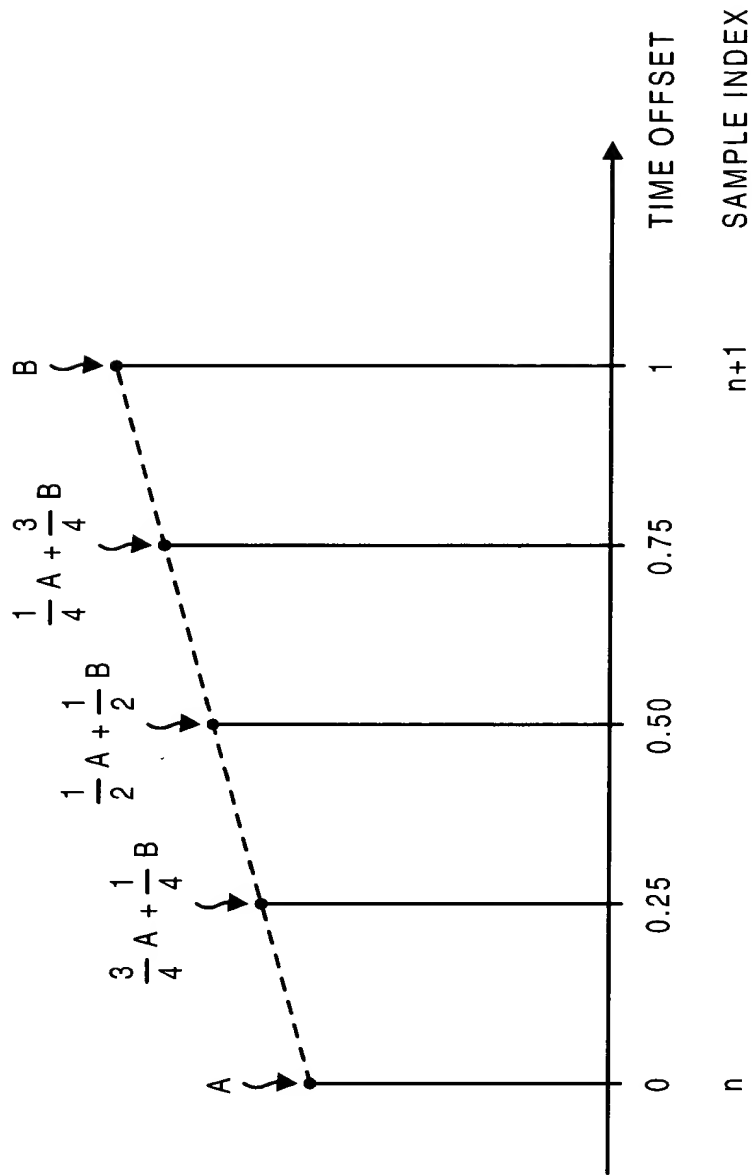


FIG. 7C

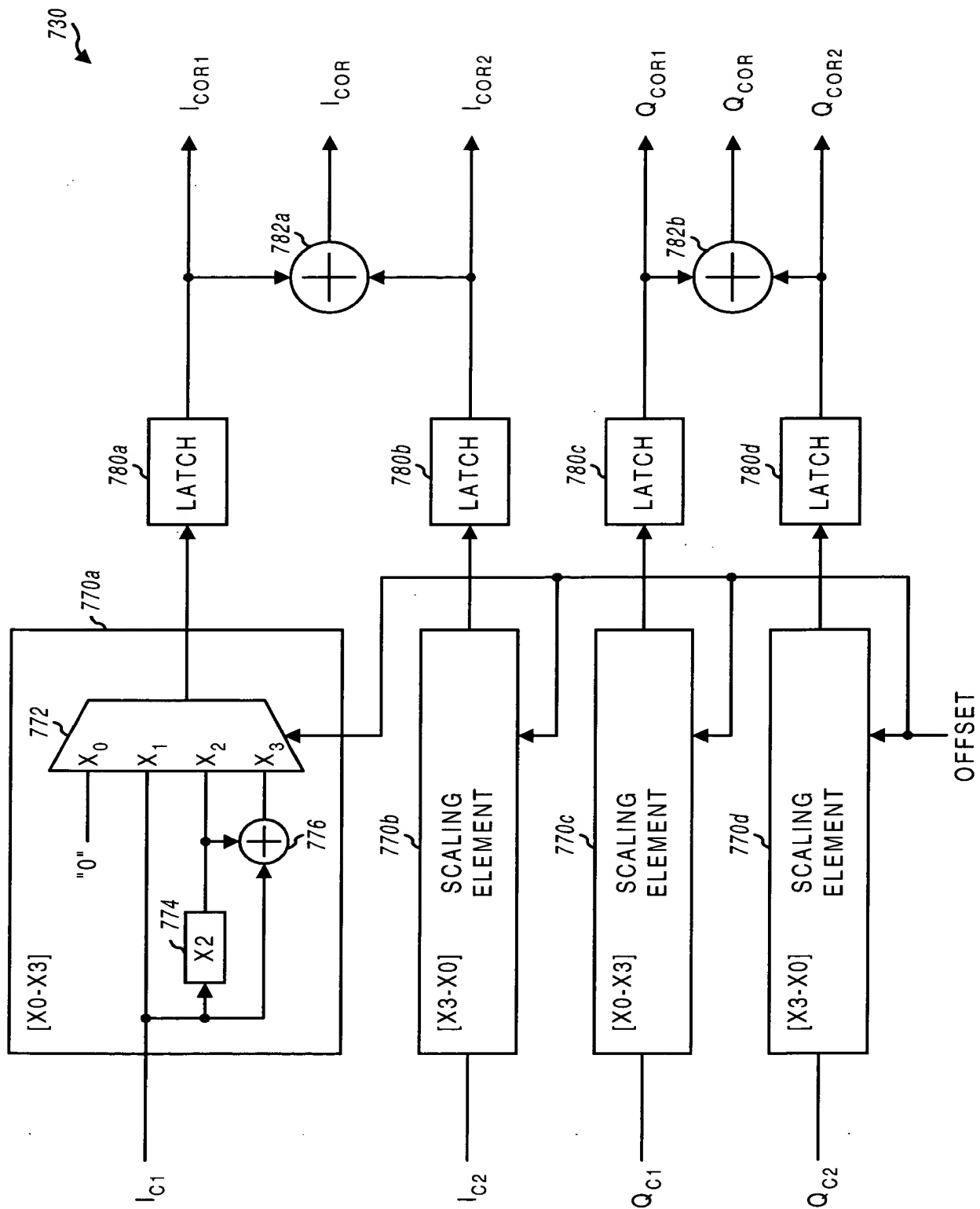


FIG. 7D

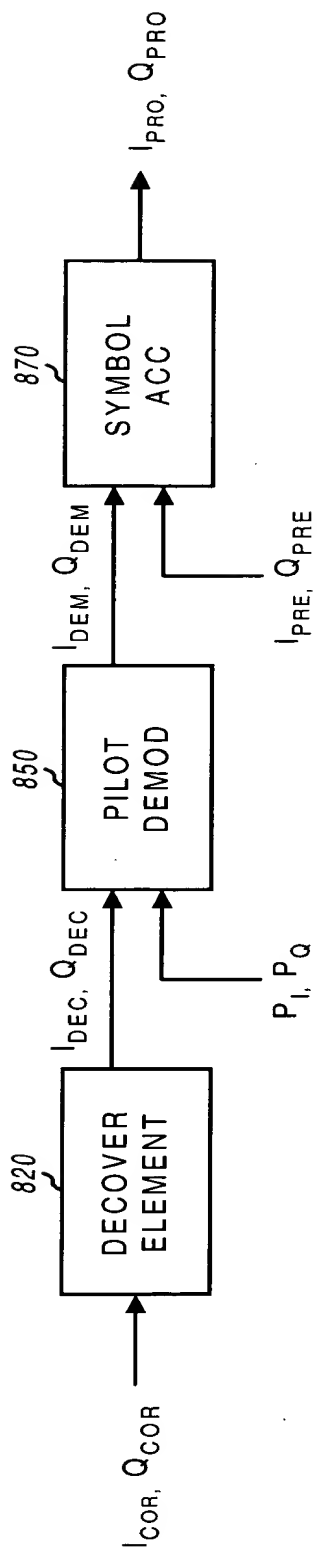


FIG. 8A

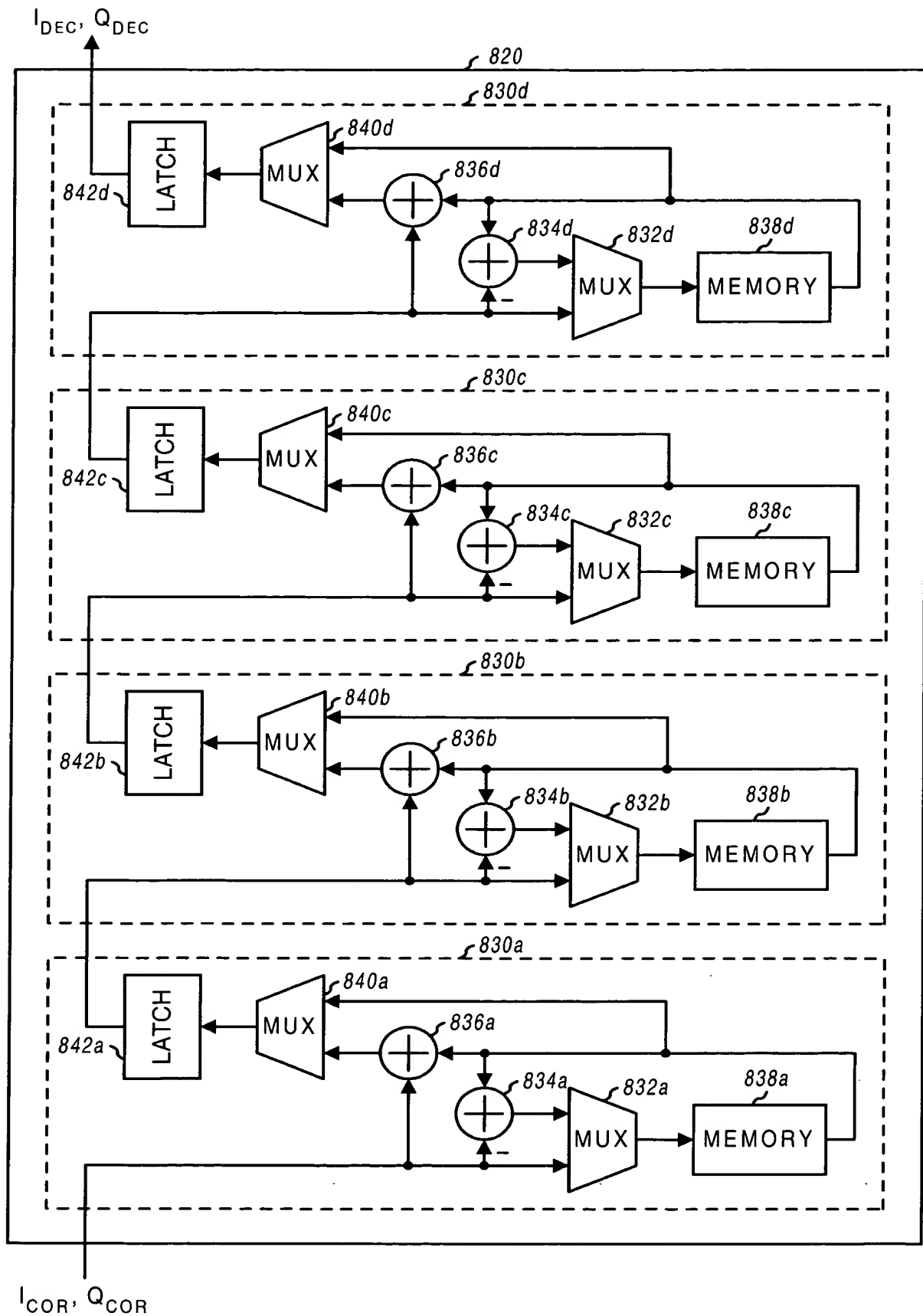


FIG. 8B

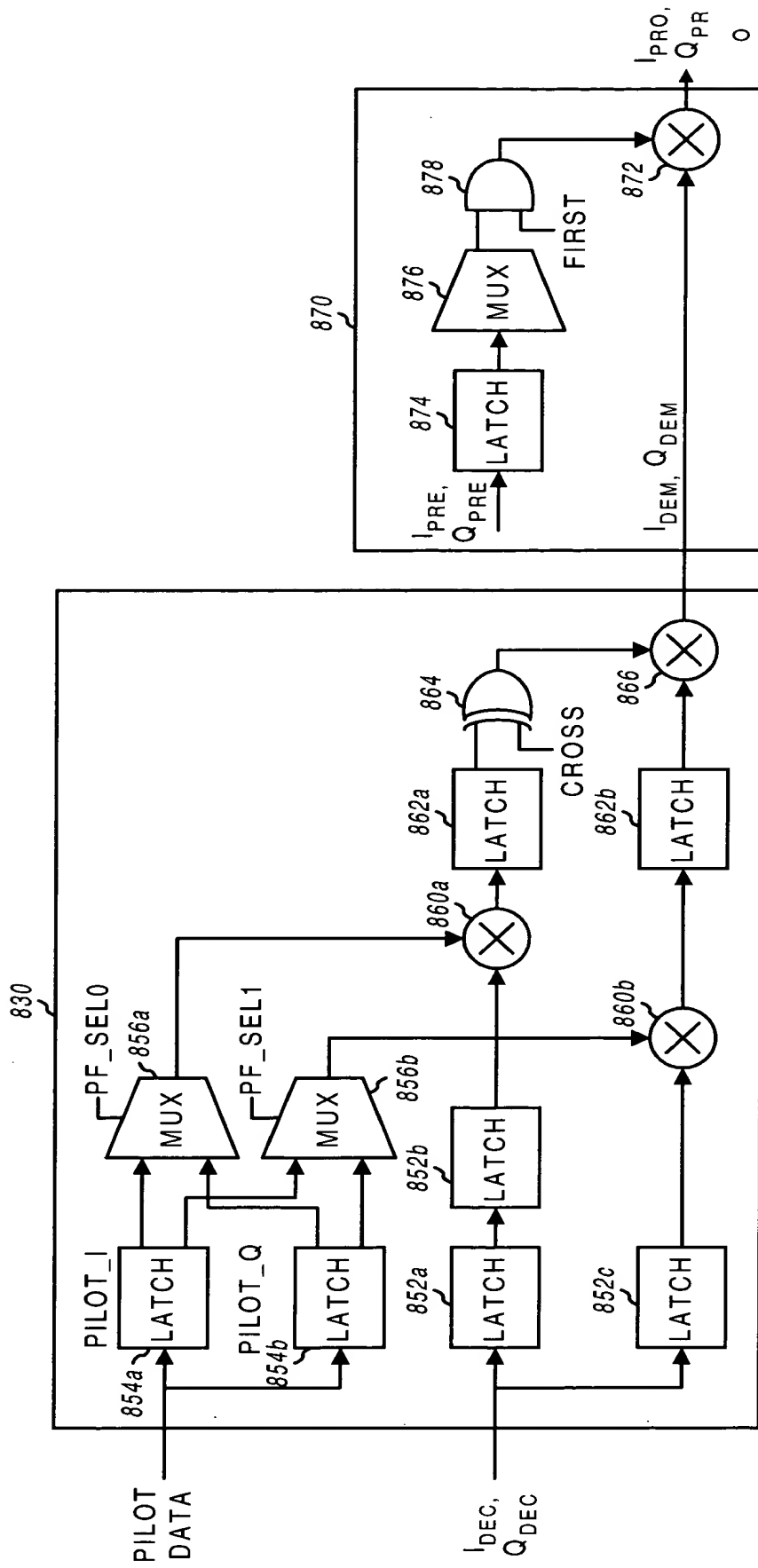


FIG. 8C

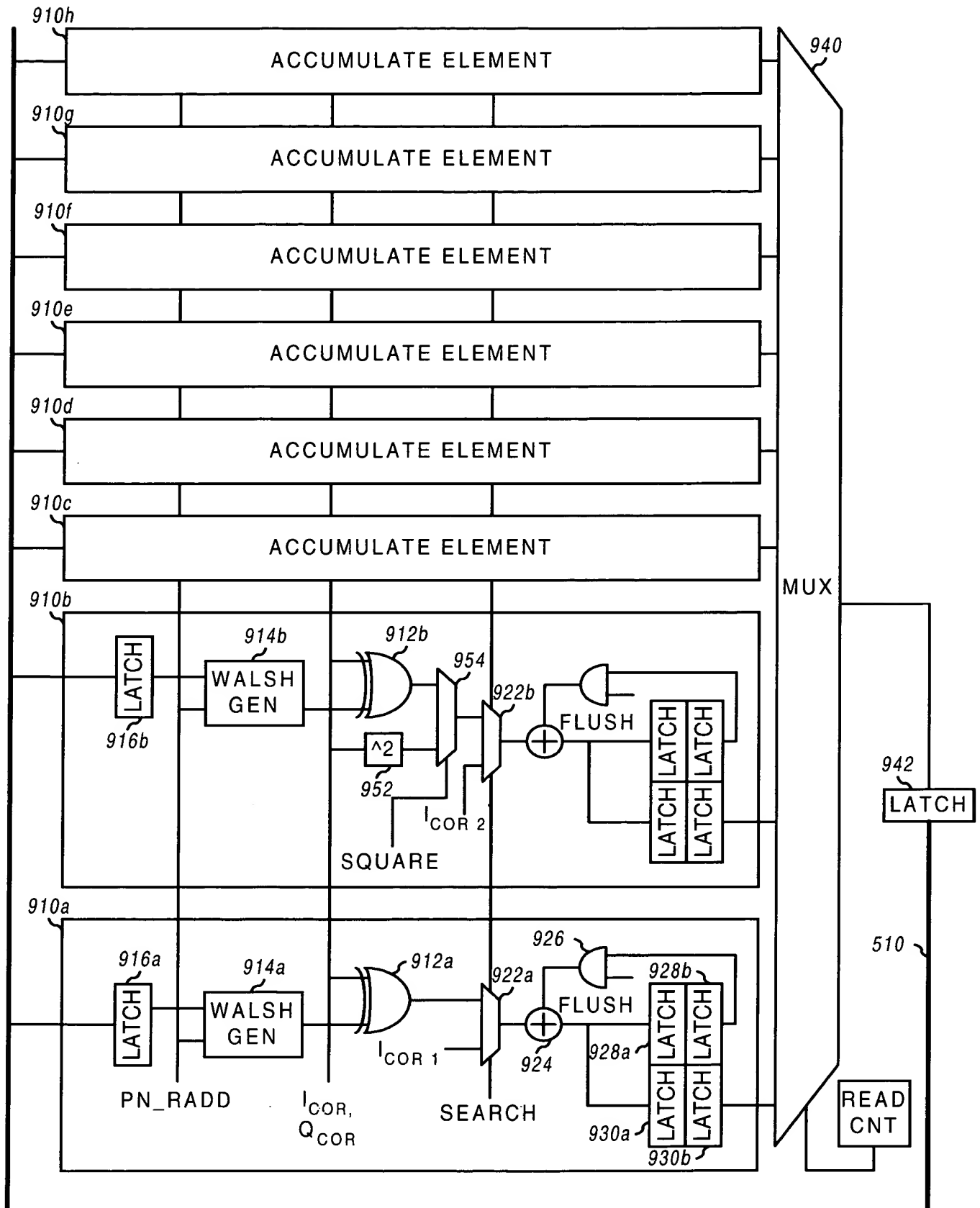


FIG. 9

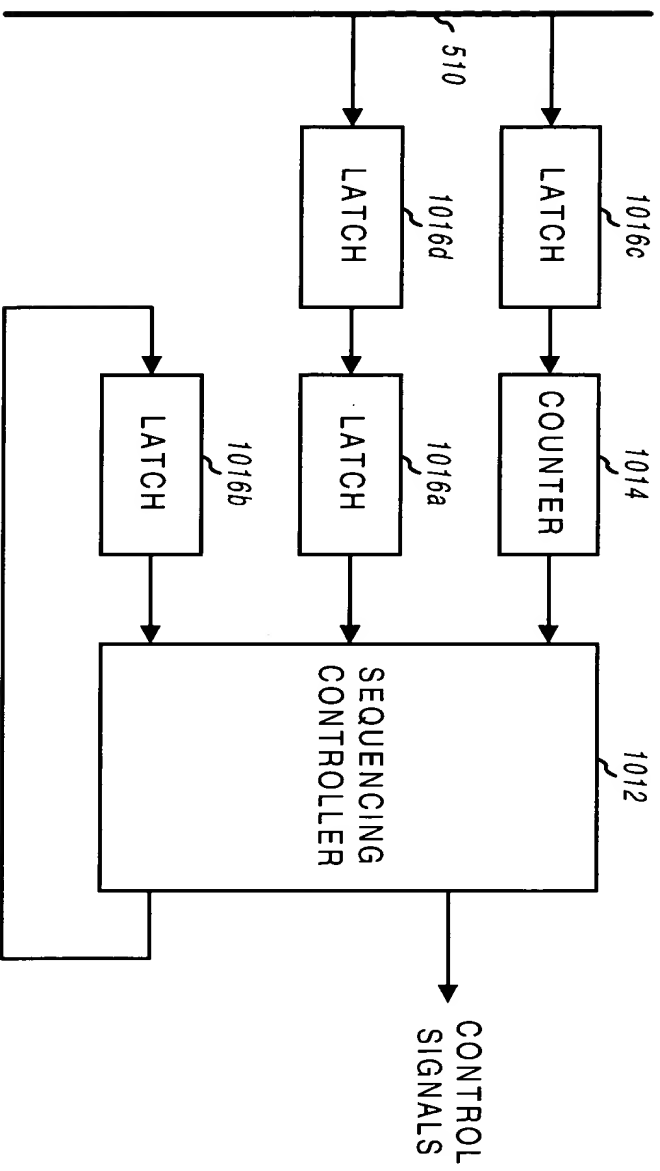
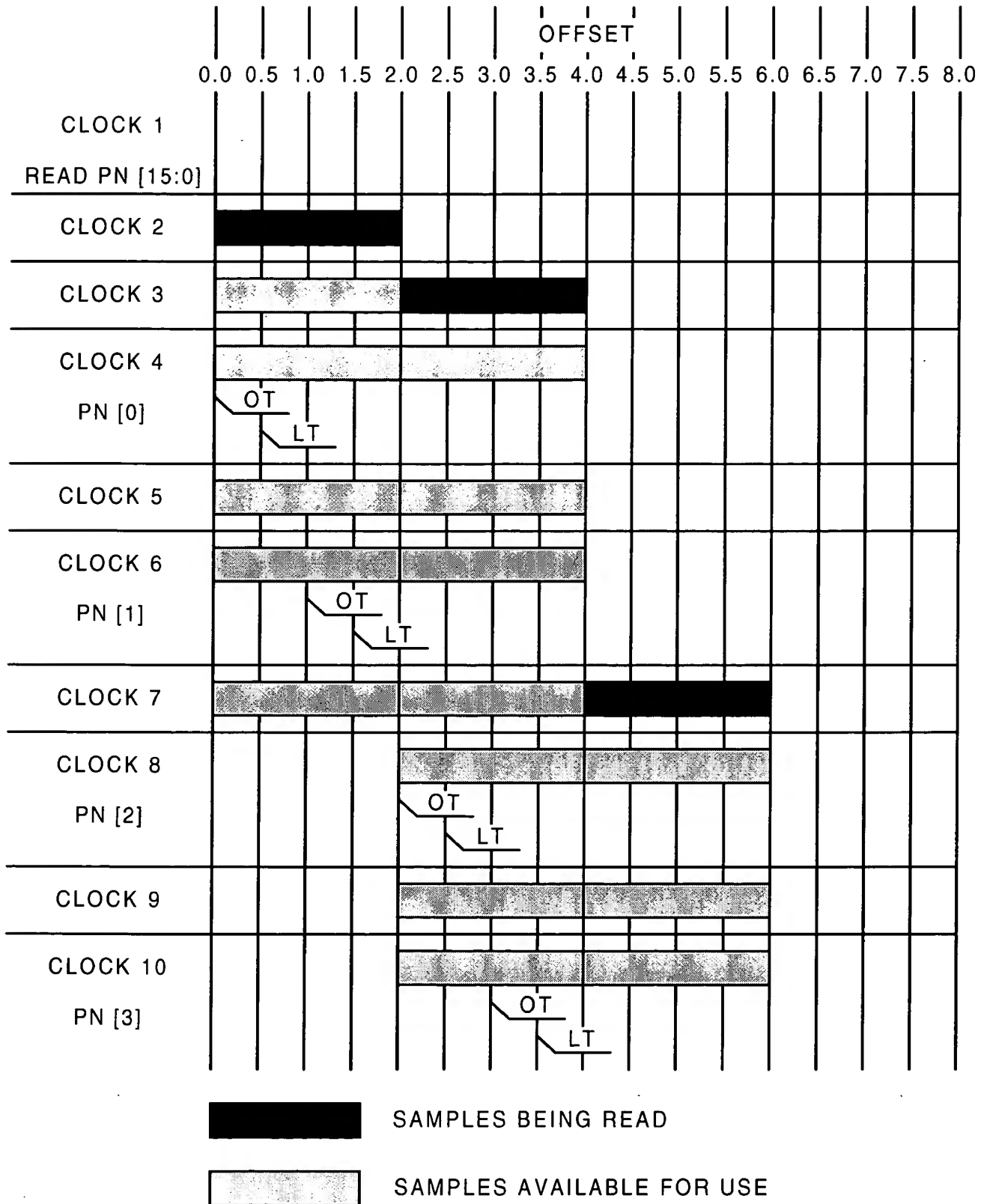


FIG. 10

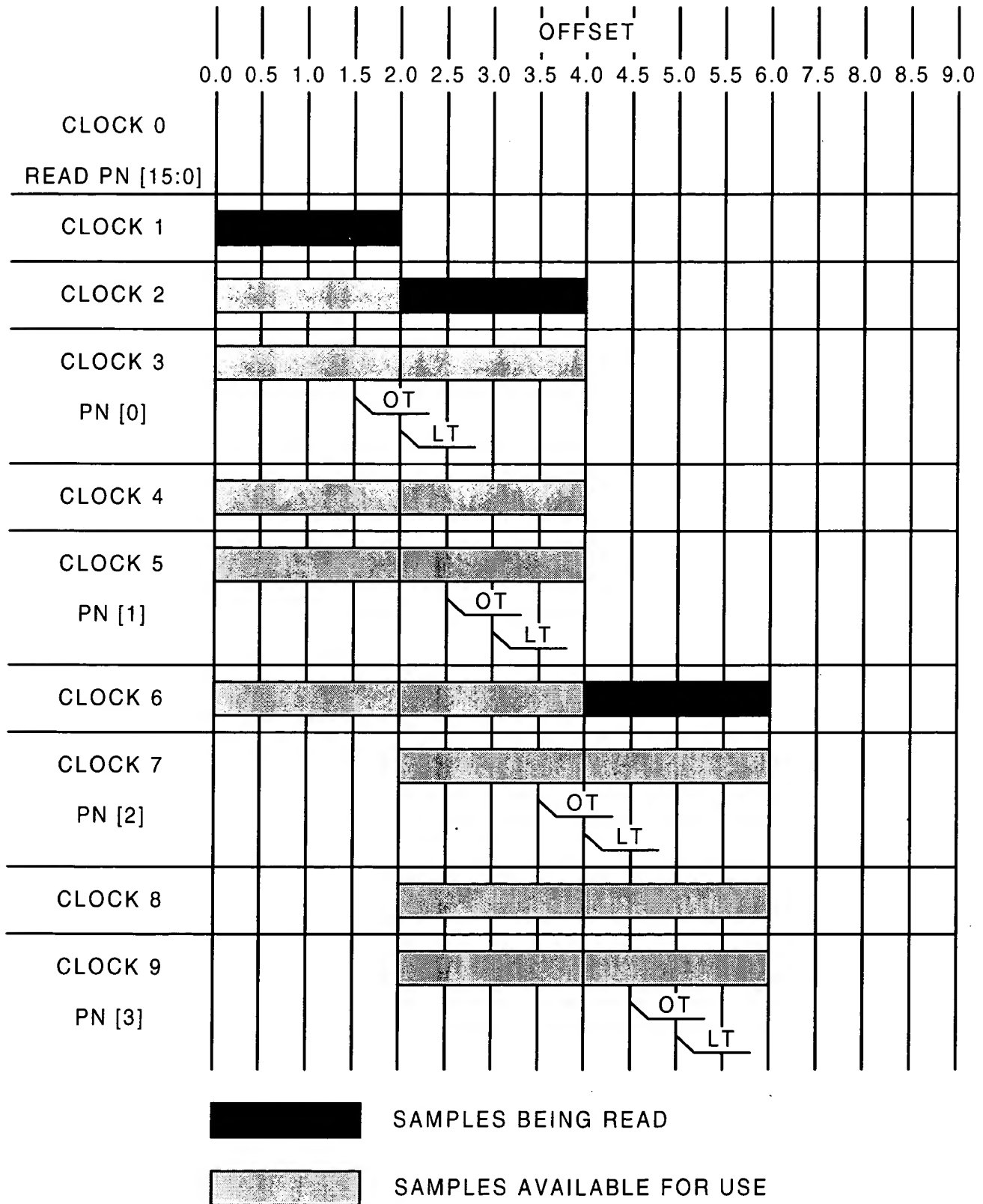


# FORWARD DATA FINGER OFFSET 0.0



**FIG. 11A**

# FORWARD DATA FINGER OFFSET 1.5



**FIG. 11B**